AKASH BAGWAN

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Professional Summary

Design Verification Engineer with industry experience at **Synopsys**, specializing in UVM-based verification of high-speed protocols **(MIPI M-PHY)**. Proven expertise in SystemVerilog, SVA, and constrained-random verification, achieving 100% functional coverage in production-grade environments. Strong in debugging complex RTL issues using VCS & Verdi, with solid foundation in AMBA protocols (APB/AHB).

Technical Skills

Verification Languages & Methodology: SystemVerilog, UVM (Universal Verification Methodology), Verilog, SVA (System Verilog Assertions),Constrained Random Verification, Functional Coverage, Assertion-Based Verification, Coverage-Driven Verification

RTL Design: Digital Design, Verilog RTL, Combinational & Sequential Logic, Finite State Machines (FSM)

Protocols: MIPI M-PHY, APB (Advanced Peripheral Bus)

EDA Tools: Synopsys VCS, Verdi, Xilinx Vivado

Programming & Scripting: C, C++, OOP (Object-Oriented Programming), Python, Shell Scripting, Linux

Professional Experience

Technical Engineering Intern (MPHY Verification) ***Apr 2025 – Apr 2026***

Synopsys, Hyderabad, India

- Contributed to **MIPI M-PHY** IP verification, validating high-speed interface functionality against protocol specifications in a production-grade UVM environment.
- Developed comprehensive **System Verilog Assertions (SVA)** targeting corner-case and boundary behaviors, directly improving verification completeness.
- Achieved **100% functional coverage**, improving verification completeness and reducing post-silicon bug.
- Developed **20+ SystemVerilog Assertions (SVA)** targeting corner cases, significantly improving bug detection efficiency
- Performed simulation, debugging, and waveform analysis using Synopsys VCS and Verdi to identify and resolve verification failures.
- Gained hands-on proficiency in complete **UVM testbench** flow: driver, monitor, scoreboard, agent, sequencer, and coverage collector components.

Design & Verification Trainee ***Jul 2024 – Mar 2025***

FutureWiz, Noida, India

- Gained in-depth knowledge of **Advanced Digital Design, Verilog, SystemVerilog, and Universal Verification Methodology (UVM)** through intensive structured training.
- Contributed to **RTL design and implementation** projects, applying efficient coding practices and simulation-driven debugging techniques.
- Developed and executed SystemVerilog testbenches for digital circuit verification, achieving comprehensive code and **functional coverage**.
- Strengthened proficiency in digital circuit simulation, waveform debugging, and verification flow using industry-standard methodologies.

Projects

APB Slave Interface Verification

- Designed and verified an **APB (Advanced Peripheral Bus)** Slave interface using Verilog, ensuring accurate protocol **implementation and functional correctness against AMBA specification**.
- Developed **constrained-random SystemVerilog testbenches**, achieving comprehensive code and **functional coverage while optimizing overall design performance**.
- Implemented complete **UVM environment** including agent, driver, monitor, scoreboard, and sequence library for protocol verification

8-Bit Arithmetic Logic Unit (ALU) — RTL Design & UVM Verification

- Designed **synthesizable 8-bit ALU RTL in Verilog** supporting arithmetic, logical, shift, and compare operations using opcode-based control logic.
- Developed a self-checking **SystemVerilog and UVM testbench**, verifying functional correctness across all operations including corner cases, via simulation and waveform analysis.

IoT-Based Smart Parking System

- Implemented embedded hardware model integrated with a cloud database; built an Android app for real-time parking slot availability monitoring.

Education

Bachelor of Technology (B.Tech) – Electronics and Communication Engineering ***Oct 2020 – Jun 2024***

IPS Academy Institute of Engineering and Science, Indore, India **GPA: 9.33 / 10.0**